**2-Bit Binary Adder Project Report**

**Introduction:**

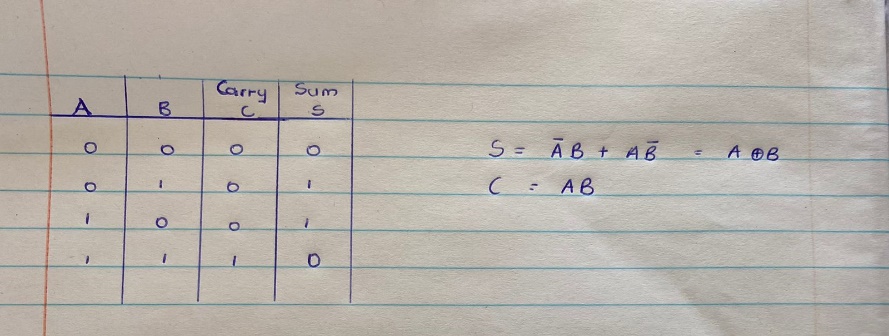
The project aims to create a digital circuit that adds 2-bit binary numbers and outputs a 3-bit binary numbers which includes the carry out. This is done by utilizing two half adders and basic digital logic gates.

**Objective:**

The goal is to design a digital circuit that has the ability to add two 2-bit binary numbers and produce a 3-bit binary sum which also includes the carry out.

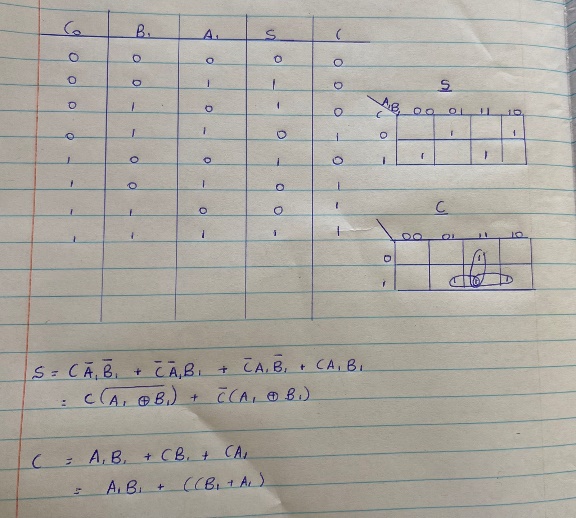
**Methodology:**

* The first half adder and the second half adder were established through the use of truth tables. The sum was implemented using XOR gates, and the carry using an AND gate.



**Figure 1.1**

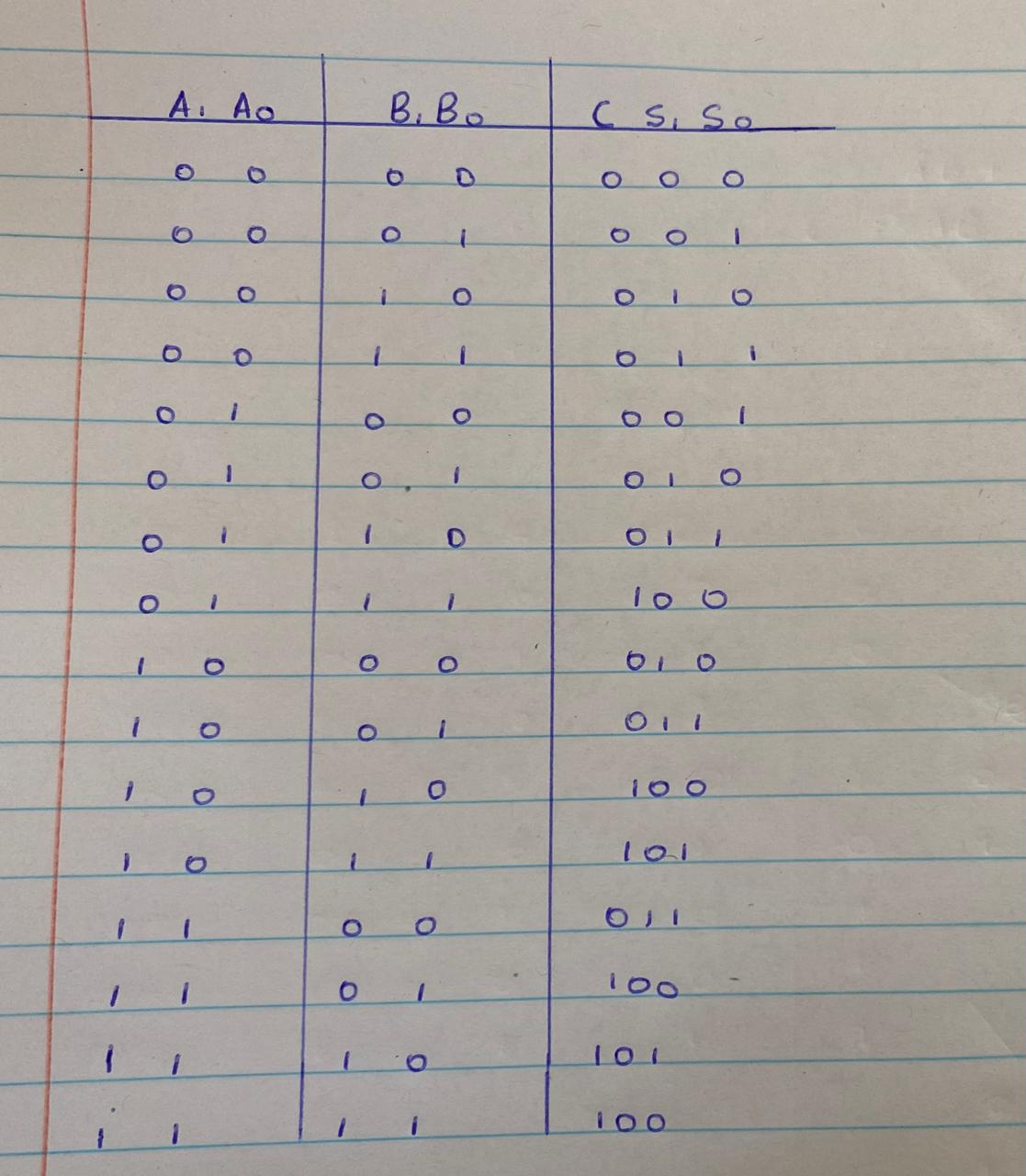
* To design the external gates, a truth table of the expected outputs was developed and the carry output was minimized using Boolean algebra and K-Maps which are minimizing techniques.



**Figure 1.2**

**Testing:**

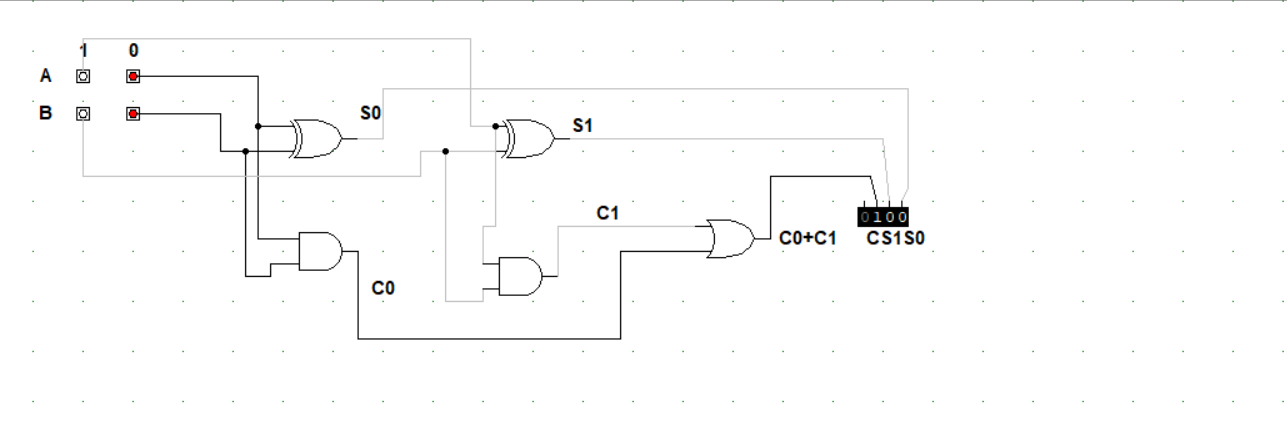
To test whether the circuit functioned correctly or not, a truth table was made showing all the possible combinations of two 2-bit binary numbers and their sums.



**Figure 1.3**

**Problems encountered:**

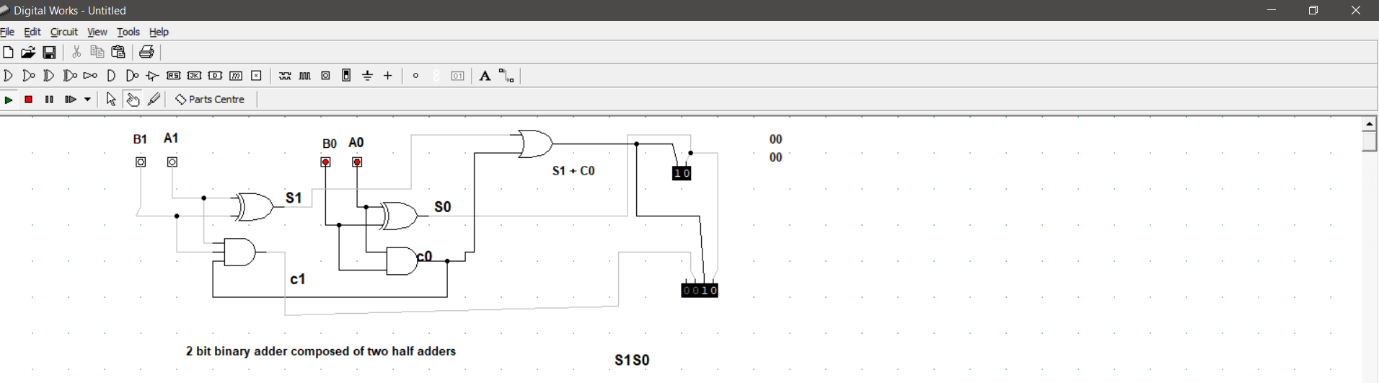
* There was an initial design where a problem was encountered with the carry out from the least significant bits of the two 2-bit binary numbers. The expected sum of the combination A0 and B0 was supposed to be 010 whereas the digital circuit gave an invalid sum of 100.



**Figure 1.4**

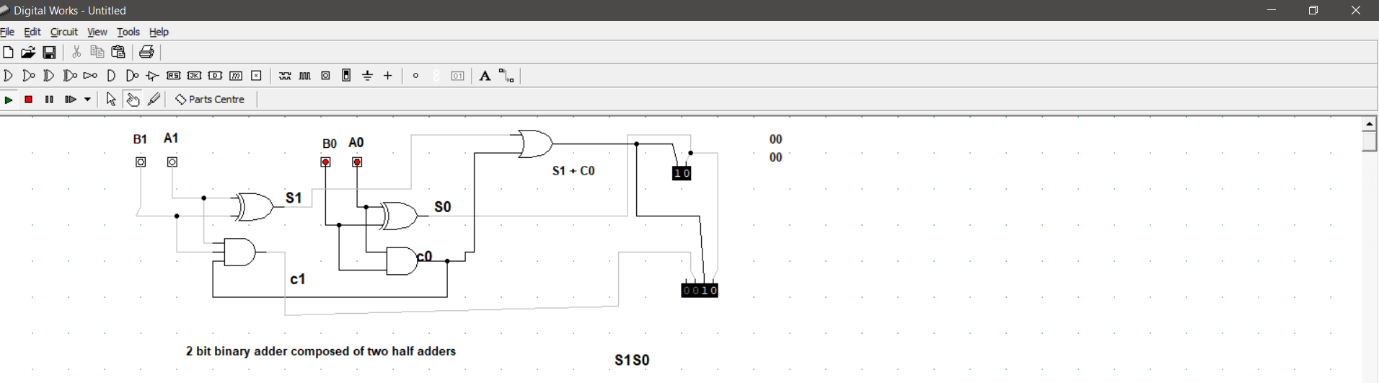
The issue was resolved by adding the carry out from the least significant bits to th

e sum of the most significant bits as shown in figure 1.5. An additional OR gate was added to the circuit which improved its functionality by adding S1 and C0.



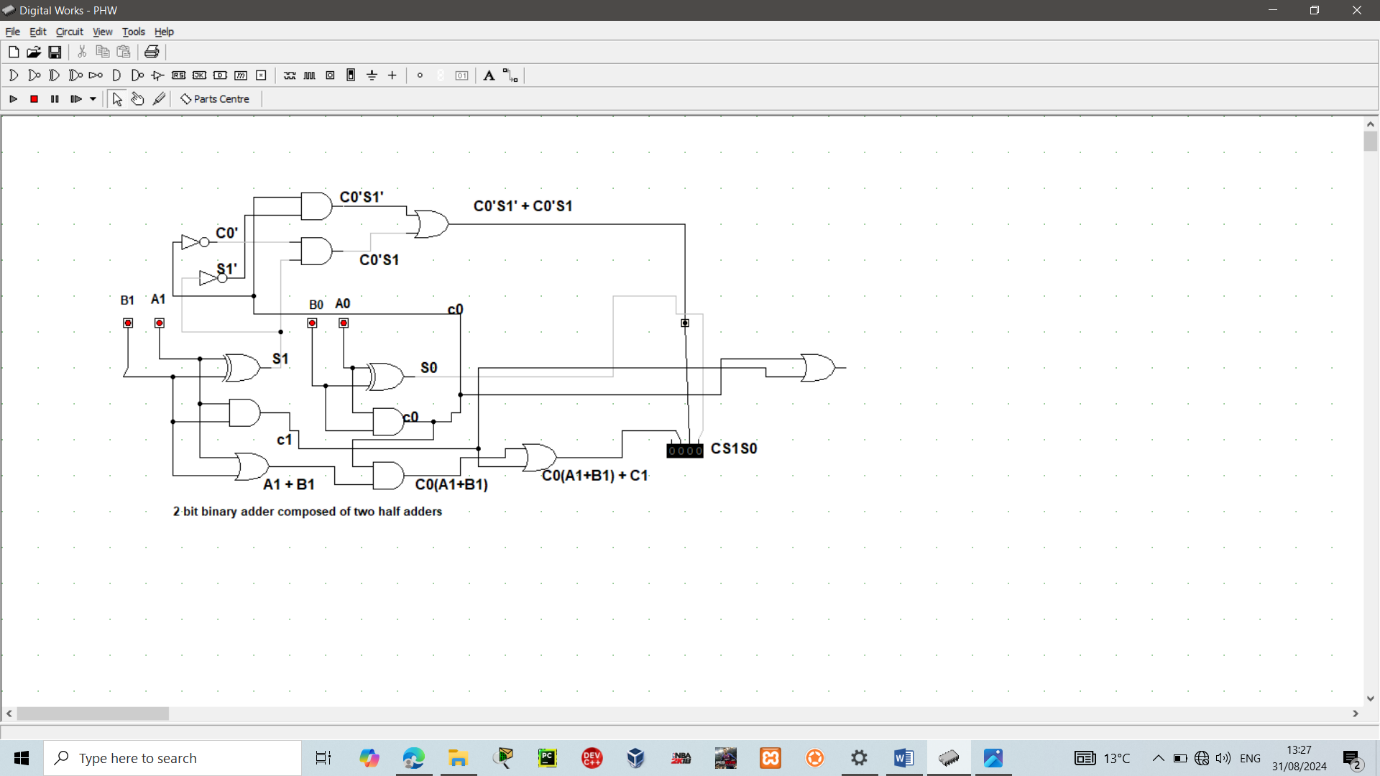
**Figure 1.5**

* However, this resolution led to another problem where the carry out from the most significant bits was not shown in the final sum.



**Figure 1.6**

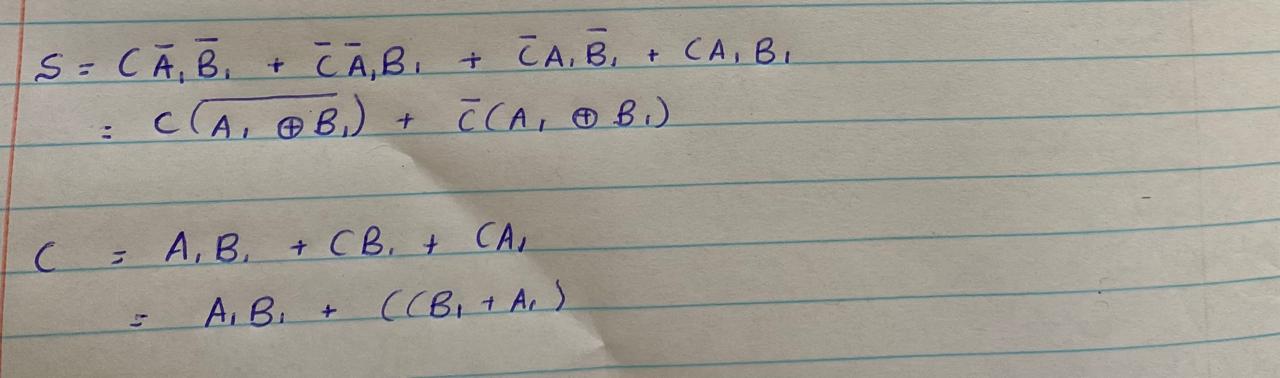
The challenge was countered by minimizing the carry out function from the truth table of the expected outcomes (see figure 1.3). This is seen in figure 1.7 through the addition of the external gates.



**Figure 1.7**

**The final solution:**

The solution of the last problem encountered was a gateway to the final result that worked for all the possible combinations in contrast to the other resolutions which did not work for all the combinations. As shown in figure 1.8, below are the Boolean expressions that led to the ultimate working result. S signifying the expression for the sum, and C for the carry out.



**Figure 1.8**